IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	No. 6:21-cv-00057-ADA [redacted]

PLAINTIFF VLSI TECHNOLOGY LLC'S OPPOSITION TO DEFENDANT INTEL CORPORATION'S RULE 50(B) RENEWED MOTION FOR JUDGMENT AS A MATTER OF LAW (D.I. 591)

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INTRODUCTION AND LEGAL STANDARD

A court may grant judgment as a matter of law ("JMOL") against a prevailing party only if "a reasonable jury would not have a legally sufficient evidentiary basis to find for the party on that issue." Fed. R. Civ. P. 50(a)(1). In deciding a renewed JMOL motion, "a 'court must draw all reasonable inferences in favor of the nonmoving party, and it may not make credibility determinations or weigh the evidence.'" *Taylor-Travis v. Jackson State University*, 984 F.3d 1107, 1112 (5th Cir. 2021). "The court 'must disregard all evidence favorable to the moving party that the jury is not required to believe.'" *Id.* "This is because '[c]redibility determinations, the weighing of the evidence, and the drawing of legitimate inferences from the facts are jury functions, not those of a judge.'" *Wellogix, Inc. v. Accenture, L.L.P.*, 716 F.3d 867, 874 (5th Cir. 2013).

"A jury verdict must stand unless there is a lack of substantial evidence, in the light most favorable to the successful party, to support the verdict." *Am. Home Assur. Co. v. United Space Alliance, LLC*, 378 F.3d 482, 487 (5th Cir. 2004). "Substantial evidence is more than a scintilla, less than a preponderance." *Nichols v. Reliance Standard Life Ins. Co.*, 924 F.3d 802, 808 (5th Cir. 2019). Thus, JMOL must denied if a jury's verdict is supported by "legally sufficient evidence that amounts to more than a mere scintilla." *Laxton v. Gap Inc.*, 333 F.3d 572, 585 (5th Cir. 2003).

I. INTEL'S MOTION FOR JMOL OF NO INFRINGEMENT SHOULD BE DENIED

A. The Jury's Infringement Verdict For The '373 Patent Is Well-Supported

1. Substantial Evidence Supports The Jury's Infringement Finding For The "Minimum Operating Voltage" Limitations

The asserted claims of the '373 patent recite limitations relating to "a value of a ***minimum operating voltage*** of the memory." PTX-4, Cl. 1; *id.*, Cl. 9 ("a memory location that stores a value representative of the minimum operating voltage"). [redacted]

[redacted]

[redacted] Dr. Conte further testified that he verified all of this by analyzing ***source code*** in the Accused Products. *See, e.g.*, 3/1 Tr. [Conte] 1451:4-1452:5 ("I examined the actual P-code. … I verified with the code that's in the PCU."). There was thus far more than substantial evidence supporting the jury's finding that the "RING_RETENTION_VOLTAGE" is "the minimum operating voltage of the C6 SRAM" memory. 2/23 Tr. [Conte] at 484:25-485:3.

Yet, Intel contends "there is no relationship between RING_RETENTION_VOLTAGE and the C6 SRAM ***specifically*** (as opposed to the ***entire*** ring domain)." D.I. 591 at 3. Intel argues that the "RING_RETENTION_VOLTAGE applies ***generally*** to the 'ring domain,' which contains multiple components beyond the C6 SRAM." *Id.* (emphasis in original). But Intel's expert confirming that RING_RETENTION_VOLTAGE is a minimum operating voltage of "parts of the

ring ***in addition to*** the C6 SRAM" (2/25 Tr. [Sylvester] 944:19-945:2) does not refute that it is the minimum operating voltage of the C6 SRAM memory, which is one of the "parts of the ring." *Id.* The '373 patent claims do not recite the word "***specifically***" as Intel suggests (D.I. 591 at 3; 2/25 Tr. [Sylvester] 944:19-945:2), nor do they bar the "minimum operating voltage of the memory" from ***also*** being the minimum operating voltage of parts ***in addition to*** the memory. PTX-4, Cl. 1. The '373 patent claims include the transition term "***comprising***" (*id.*), and it is black-letter law that "[t]he transitional term 'comprising' . . . is inclusive or open-ended and does not exclude additional, unrecited elements." *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005).

[redacted] Dr. Conte explained "RING_RETENTION_VOLTAGE" applies to both the "LLC" and "C6 SRAM" memories, as they have "the same memory cells." 2/23 Tr. [Conte] at 483:19-485:5. It is thus "the minimum operating voltage of the C6 SRAM." *Id.* at 484:25-485:3.

Intel next argues no reasonable jury could find that the RING_RETENTION_VOLTAGE is the "minimum operating voltage" because Intel's witnesses offered unsupported competing testimony—that Dr. Conte addressed and rebutted—alleging that "the C6 SRAM … operate[s] below RING_RETENTION_VOLTAGE." D.I. 591 at 3-4. Intel employs rhetorical sleight of hand in its brief, arguing that "the RING_VF_VOLTAGE_0 ***fuse*** value … is indisputably below the RING_RETENTION_VOLTAGE ***voltage*** value." *Id.* at 5. In doing so, Intel glosses over the factual dispute as to whether the ring ***operates*** at the "RING_VF_VOLTAGE_0 ***fuse*** value" (*id.*), as opposed to at a higher operating voltage level that is ***derived from*** that fuse value after ***inverse temperature dependence ("ITD") compensation*** calculations are applied at runtime.

Notably, Intel misrepresents testimony by Dr. Conte, alleging that "Dr. Conte admitted that the RING_VF_VOLTAGE_0 fuse value … ***reflects*** a voltage that is ***'actually used'*** in the accused products." D.I. 591 at 5. Not so. Dr. Conte agreed that "RING_VF_VOLTAGE_0, which you just talked to Mr. Heinrich about, does, in fact, ***correspond to*** a voltage level ***actually used***." 3/1 Tr. [Conte] 1436:21-1437:7. That was both accurate and consistent with his other testimony, as the RING_VF_VOLTLAGE_0 fuse value does "correspond to" a higher operating voltage level "actually used" that is derived from the fuse value at runtime by applying ITD compensation.

The jury was free to reject Intel's theory and to credit Dr. Conte, as the record contains substantial evidence that the ***operating voltage*** derived from the RING_VF_VOLTAGE_0 ***fuse*** value is higher than the RING_RETENTION_VOLTAGE (the "minimum operating voltage"). Importantly, Dr. Conte testified that ***Intel's witnesses improperly failed to account for ITD compensation in comparing RING_VF_VOLTAGE_0 to RING_RETENTION_VOLTAGE***. *See* 3/1 Tr. [Conte] 1425:1-1432:5, 1434:9-1437:7, 1450:8-1452:12. As such, Intel's witnesses failed to "compar[e] them on an apples-to-apples basis at the same temperature," thus yielding incorrect results because RING_VF_VOLTAGE_0 "is measured at ***100 degrees Celsius***" whereas "RING_RETENTION_VOLTAGE is measured at ***zero degrees Celsius***." *Id.* at 1429:13-20. Dr. Conte explained that the Accused Products "calibrate those voltage levels to the same temperature" at runtime by applying ITD compensation, and that "***[w]hen you compensate for temperature, V0 is going to be always above the RING_RETENTION_VOLTAGE***." *Id.* at 1429:21-1431:22; *see also, e.g.*, *id.* at 1450:8-1452:12 ("When you compensate them with [the ITD] equations that were in that very document we were looking at, you'll end up with V0 always above RING_RETENTION_VOLTAGE."). Tellingly, Intel does not even attempt to deny in its brief that its witnesses "failed to account for 'inverse temperature dependence' … in comparing the values

of RING_RETENTION_VOLTAGE and RING_VF_VOLTAGE_0." D.I. 591 at 4. Intel instead tries to dodge this undisputed fact with a conclusory statement alleging that "Dr. Conte provided no factual support for this claim." *Id.* Not so. Intel's vague non-denial plainly ignores the record.

First, Dr. Conte explained that his testimony was supported by multiple Intel documents. For example, Dr. Conte directed the jury to an Intel specification which, consistent with his testimony, [redacted] D-505 at 24 (shown right, emphasis added); *see* 3/1 Tr. [Conte] 1425:1-1426:20. Dr. Conte also discussed Intel specifications PTX-3662 and PTX-3851 which, consistent with his testimony, state: [redacted] PTX-3662.702; PTX-3851.1280; 3/1 Tr. [Conte] 1431:2-22.[1]

Second, Dr. Conte testified that he also confirmed both his testimony and Intel's documents by reviewing the ***actual source code*** in the Intel Accused Products. 3/1 Tr. [Conte] 1451:4-1452:5 (explaining that he "examined the actual P-code" and "did not" rely solely on Intel documents).

Third, Dr. Conte explained that his testimony was also supported by code he wrote himself. Referencing D-1107A, he testified: "***I wrote this code*** because Intel gave us this complicated encoded database of millions of entries, and I had to write code to decode that so I could analyze it." 3/1 Tr. [Conte] 1428:11-21. Dr. Conte explained that Intel's expert Dr. Sylvester had taken the code and used it to compare RING_RETENTION_VOLTAGE to RING_VF_VOLTAGE_0, but that ***"[h]e misinterpreted it"*** by failing to apply ITD compensation. *Id.* at 1428:22-1430:23.

[1] Intel's suggestion that an exhibit should be disregarded if it is a "draft document and 'not a final description of the products'" is meritless. D.I. 591, Intel Br. at 4. Intel cites no authority for this, and any such rule would make no sense, as documents are rarely "final" product descriptions. 3/1 Tr. [Conte] 1435:20-23 ("I believe virtually all the documents Intel produced were drafts.").

Fourth, the jury had good reason to credit Dr. Conte's testimony over that of Intel's expert Dr. Sylvester, who was impeached on cross-examination. Dr. Sylvester had testified that the median ***RING_RETENTION_VOLTAGE*** value was ***0.75 volts*** and that the median ***RING_VF_VOLTAGE_0*** value was lower at ***0.6172 volts*** (without applying ITD compensation). 2/5 Tr. [Sylvester] 946:9-948:3. Dr. Sylvester contended "this is clear evidence that the RING_RETENTION_VOLTAGE is not a minimum retention voltage." *Id.* at 948:4-8. But on cross, he was questioned regarding an Intel document [redacted] showing that "***Vmin***" of the "***C6SRAM***" is "***0.75***" ***volts***, the exact voltage Dr. Sylvester had identified for the RING_RETENTION_VOLTAGE. PTX-3675.1 (above, emphasis added); *see* 2/5 Tr. [Sylvester] 985:12-989:9. He confirmed the "0.75" volt "Vmin" is "***a minimum voltage***." *Id.* at 985:16-24.[2]

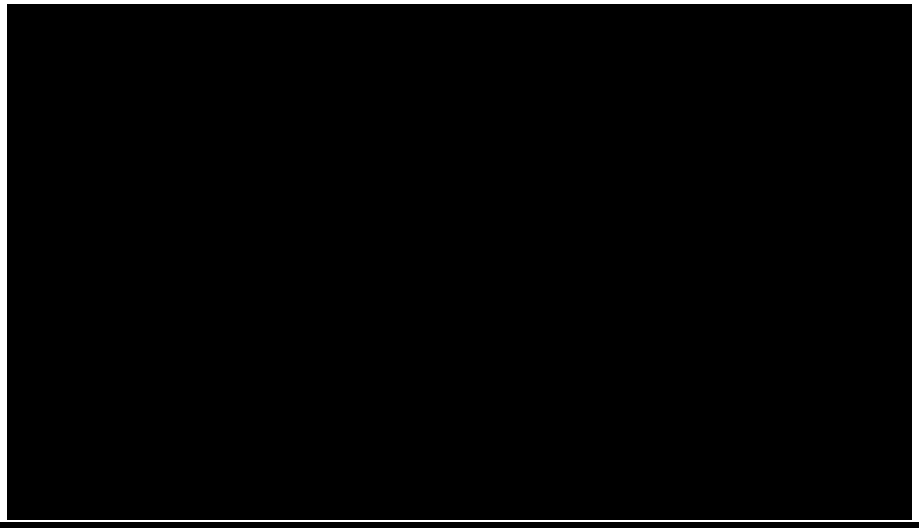
Ultimately, this dispute "boil[ed] down to a question of credibility, and the jury believed [VLSI's expert Dr. Conte] over [Intel's witnesses]." *Arismendez v. Nightingale Home Health Care, Inc.*, 493 F.3d 602, 608 (5th Cir. 2007) (reversing JMOL ruling). "[T]he jury believed [Dr. Conte], and there is [far] more than a scintilla of evidence to support the jury verdict." *Id.* at 609.

2. Substantial Evidence Supports The Jury's Infringement Finding For The "When" Limitations

The claims recite limitations such as "providing the first regulated voltage … ***when*** the first regulated voltage is ***at least*** the value of the minimum operating voltage," and "providing the second regulated voltage … ***when*** the first regulated voltage is ***less than*** the value of the minimum operating voltage." PTX-4, Cl. 1. VLSI offered substantial evidence that these limitations are met.

[2] Intel also says "VLSI offered no evidence that any minimum operating voltage for the C6 SRAM is 'determined,' through testing or otherwise." D.I. 591, Intel Br. at 5 n.6. Not so. [redacted]

[redacted]



[redacted]

This all provided far more than substantial evidence to support the verdict.

Yet, Intel argues that "the RING_RETENTION_VOLTAGE fuse value is [not] ever ***used to guide*** 'when'" voltages are supplied and "is not ***used as part of*** the accused voltage-switching functionality." D.I. 591 at 6. This argument is baseless. The claims recite providing a voltage "***when***" a condition is present—*e.g.*, "***when*** the first regulated voltage ***is at least*** the value of the minimum operating voltage." PTX-4, Cl. 1. Contrary to Intel's suggestion, the claims do not require that the minimum operating voltage be ***"used to guide"*** or ***"used as part of"*** anything (whatever Intel means by that). D.I. 591 at 6. [redacted] To the extent Intel seeks a new construction, it has "waive[d] [any] right to present new claim construction disputes … for the first time after

trial." *Lazare Kaplan Int'l v. Photoscribe Techs.*, 628 F.3d 1359, 1376 (Fed. Cir. 2010). [redacted]

[redacted]

[redacted]

3. Substantial Evidence Supports The Jury's Infringement Finding For The "First Regulated Voltage" And "Functional Circuit" Limitations

The '373 patent asserted claims recite limitations such as "while the second regulated voltage is provided as the operating voltage of the memory, the ***first regulated voltage*** is provided to the ***functional circuit***." PTX-4, Cl. 1; *see id.*, Cl. 9 ("wherein while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage"). Intel contends these limitations are not met because, in its view, "during the Package C7 sleep state … VCCR voltage (what VLSI accuses as the 'first regulated voltage') is ***un***regulated and the components on the ring are ***inoperable***." D.I. 591 at 7 (emphasis in original). Intel's JMOL motion is meritless.

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted] *see also* 2/25 Tr. [Douglas] 870:20-872:25, 876:17-877:17, 877:22-878:6 (Intel engineer Jonathan Douglas explaining that FIVR ramping is deliberate and programmed, and is not instantaneous); PDX4.92-PDX4.98; PTX-1588-NAT.39-40. There was thus farm more than substantial evidence to support the infringement verdict, and the jury was free to credit Dr. Conte and the Intel testimony and documents that supported him.

B. The Jury's Infringement Verdict For The '759 Patent Is Well-Supported

1. Substantial Evidence Supports The Jury's Infringement Finding For The "Request" Limitation

JMOL is inappropriate if the record evidence is such that "reasonable and fair-minded men in the exercise of impartial judgment might reach different conclusions." *Laxton*, 333 F.3d at 579. Here, VLSI presented both literal and doctrine of equivalents ("DoE") infringement theories on the '759 patent's "request" limitation. And while the jury here found in VLSI's favor on DoE, there was substantial evidence sufficient for a reasonable jury to find either literal or DoE infringement.

Regarding literal infringement, Intel contends that "no reasonable jury could have found the 'request' limitations literally met … because the Core_Active signal … is not an input to the [PCU's] autonomous algorithms that are used to change the clock speed." D.I. 591 at 11 n.11. Intel argues that the "Core_Active" signal is not a "***request***," but rather that, "[a]t best, the Core_Active signal is one ***datapoint*** among many pieces of information that are monitored [by the PCU] to determine the frequency in Intel's products." *Id.* Intel's argument is meritless. [redacted] Intel's argument that the "Core_Active" signal is merely a "datapoint" that is "monitored" by the PCU is mere semantics, is contrary to the plain meaning of the term "request," and was refuted by the testimony of Intel's own expert Dr. Grunwald. *See, e.g.*, 2/26 Tr. [Grunwald] 1242:19-1252:4 (discussing analogy to "customers in a restaurant," and agreeing that a "request" can be either (a) an "explicit" or "direct command" like "check, please," or (b) a non-explicit "statement of a condition," like "I don't have any silverware"). Thus, notwithstanding this particular jury's verdict, VLSI presented substantial evidence sufficient for a reasonable jury to find literal infringement.

Substantial evidence likewise supported this jury's DoE infringement verdict. In arguing for JMOL on DoE, Intel mischaracterizes Dr. Conte's testimony. Intel suggests Dr. Conte testified that "C0 residency information is not sent 'in response to a predefined change in performance' in the Intel products," but rather that "C0 residency counters 'are sampled periodically'" without regard to when a change in performance occurs. D.I. 591 at 10. Intel also cites out of context to Dr. Conte's testimony that "periodic reading of information is not a request." *Id.* Intel's assertions are misleading. Dr. Conte testified that the ***Core_Active*** signals ***are not*** sent periodically, but rather are sent whenever the core becomes active. 2/23 Tr. [Conte] 488:4-7 ("Q. Are Core_Active signals sent periodically? A. No. Q. When are they sent? A. They're sent whenever the core becomes active."). Dr. Conte further testified that his general testimony about ***periodic*** signals ***does not apply*** to the ***Core_Active*** requests. *Id.* at 488:4-10 ("Q. So does any of that testimony about periodic signals apply to the Core_Active requests? A. No."). [redacted]

Intel next contends that "Dr. Conte's equivalents theory is inconsistent with the claim, which requires the 'request' to be (1) 'provide[d]' or 'sent' by the 'first master device' and (2) 'receive[d]' by the 'clock controller.'" D.I. 591 at 10. Intel argues that "nothing in the claims

allows for the ***same component***—here, ***the PCU***—to both 'provide' (or 'send') ***and*** 'receive' the claimed 'request.'" *Id.* at 11. Intel's argument is meritless, for multiple reasons.

First, Intel misstates Dr. Conte's testimony. Dr. Conte did not opine that the "same component," or that "the PCU," both provides (or sends) and receives the claimed "request." *Id.*

[redacted]

Second, to the extent Intel contends the "first master device" and "programmable clock controller" must always comprise ***entirely separate and distinct circuits***, Intel would be seeking a new (and incorrect) claim construction, which it has waived. *See Lazare Kaplan*, 628 F.3d at 1376.

This argument also is contrary to Federal Circuit law, even for literal infringement. *See Linear Tech. Corp. v. ITC*, 566 F.3d 1049, 1055 (Fed. Cir. 2009) (claimed "second circuit" and "third circuit" do "***not require entirely separate and distinct circuits***," and absent any contrary "specific structural requirement," the "'second' and 'third' circuits must only perform their stated functions."). This is doubly true for DoE infringement, as the Federal Circuit has held that "[t]he doctrine of equivalents ***does not require a one-to-one correspondence*** between the accused device and that disclosed in the patent." *Intel Corp. v. ITC*, 946 F.2d 821, 832 (Fed. Cir. 1991). Because "[o]ne-to-one correspondence of components is not required, [the] elements or steps may be combined without ipso facto loss of equivalency." *Ethicon Endo-Surgery, Inc. v. U.S. Surgical Corp.*, 149 F.3d 1309, 1320 (Fed. Cir. 1998). "[W]hen separate claim limitations are combined into a single element of the accused device, … the doctrine of equivalents may still apply if the differences are insubstantial." *Eagle Comtronics v. Arrow Commc'ns Labs*, 305 F.3d 1303, 1317 (Fed. Cir. 2002).

Intel also failed to raise the foregoing theory in its Rule 50(a) motion. *Compare* D.I. 591 at 11 (arguing "nothing in the claims allows for the same component—here, the PCU—to both 'provide' (or 'send') and 'receive' the claimed 'request'"), *with* D.I. 551 at 6-9 (no such argument). "By not raising this argument at trial or in its Rule 50(a) motion, [Intel] has waived its right to bring a Rule 50(b) motion on this ground." *In re Isbell Records*, 774 F.3d 859, 867 (5th Cir. 2014).[3]

2. Substantial Evidence Supports The Jury's Infringement Finding For The "Provide … As An Output To Control" Limitations

The asserted claims of the '759 patent recite limitations such as the following limitations in claim 14 (claim limitation numbers added for ease of reference):

> [c] a programmable clock controller … including instructions to:
> . . . .

[3] Intel also notes the bench-trial issues "in Intel's '759 Bench Trial Brief." D.I. 591, Intel Br. at 9-10 & n.9. A Rule 50 motion on bench-trial issues is improper for the reasons noted in Part I.C below. VLSI's Opposition to Intel's '759 Bench Trial Brief is being filed concurrently herewith.

[e] ***provide*** the clock frequency of the high-speed clock ***as an output to control*** a clock frequency of a second master device …; and

[f] ***provide*** the clock frequency of the high-speed clock ***as an output to control*** the variable clock frequency of the bus ….

PTX-5, Cl. 14; *see also id.*, Cl. 18 ("output a clock frequency of a high-speed clock to control the variable clock frequency of the bus and to control a clock frequency of a second master device"). VLSI offered substantial evidence that these limitations are met.

[redacted]

[redacted]

[redacted]

There is no dispute that the Accused Products include the above functionality. Yet, Intel advances non-infringement theories that ignore both the claim language and well-settled law.

First, Intel contends the Accused Products don't infringe because "the cores and the bus run on ***different*** clock frequencies." D.I. 591 at 12 (emphasis in original). But the claims do not require that the controlled clocks have the same frequency. Indeed, they allow for different frequencies: "a ***clock frequency*** of a ***second master device***," and "the ***variable*** ***clock frequency*** of the ***bus***." PTX-5, Cl. 14; *id.* at 4:39-41 (noting the "high speed clock" for the bus "may be further adjusted"). Indeed, Intel's expert Dr. Grunwald conceded the claims include "no language" requiring the two controlled clocks to "always have the same clock frequency." 2/26 Tr. [Grunwald] 1297:13-22.

Second, Intel says "the ***same*** clock frequency must be 'output to control' both the second master device and the bus." D.I. 591 at 13 (emphasis in original). This is a red herring. [redacted]

Third, Intel argues that the high-speed clock "***is not output to*** either the ***second master device*** or the ***bus***—it is ***output to*** the '***CPLL***' and '***separate [bus] PLL***,' respectively—and the different clock frequencies output by those separate PLLs control the second master device and the bus." D.I. 591 at 13. But Intel rewrites the claims. Contrary to its suggestion, the claims do not require the "high-speed clock" to be ***output to*** the "second master device" or "bus." *Id.* They recite providing "the high-speed clock ***as an output to control a clock frequency of*** a second master device" and "***as an output to control the variable clock frequency of*** the bus." PTX-5, Cl. 14. The claims do not prohibit the use of intermediate components in effectuating that control.

Ultimately, Intel arguing non-infringement based on the "CPLL" and "separate PLL" is contrary to law. The claims use "[t]he transitional term '***comprising***,'" which "is inclusive or open-ended and ***does not exclude additional, unrecited elements***." *CollegeNet*, 418 F.3d at 1235; *see also Tech. Consumer Prods. v. Lighting Sci. Grp.*, 955 F.3d 16, 22 (Fed. Cir. 2020) (claims reciting "heat sink" did "not suggest … there must be only one heat sink," as "the 'comprising' language in the preamble suggests that there may be additional unrecited elements"). Intel's expert Dr. Grunwald agreed that "a system comprising" in the claims means that, "as long as all of the elements in the claim are present, the fact that one is adding additional features or elements would not change the question of whether a product infringes." 2/26 Tr. [Grunwald] 1282:12-1283:14.

C. Intel's Motion For JMOL On Claims Not Argued At Trial Should Be Denied

Intel seeks JMOL of no induced or contributory infringement (D.I. 591 at 13-14), and non-infringement as to claims 12 and 16 of the '373 patent and claims 1 and 26 of the '759 patent (*id.* at 2 n.3, 8 n.7), despite that VLSI did not assert these claims at trial. Intel's motion is improper. "Federal Rule of Civil Procedure 50 is clear that relief under this Rule may be appropriate only '***[i]f a party has been fully heard on an issue during a jury trial***.'" *Rembrandt Wireless Techs., LP v. Samsung Elecs.*, 2016 WL 633909, at *5 (E.D. Tex. Feb. 17, 2016) (emphasis in original);

see also C R Bard Inc. v. AngioDynamics, 979 F.3d 1372, 1380 (Fed. Cir. 2020) ("Rule 50 provides that JMOL against a party is only appropriate once the party 'has been fully heard on an issue.'").

II. INTEL'S MOTION FOR JMOL OF INVALIDITY SHOULD BE DENIED

Intel did not challenge the '373 patent's validity at trial, and for the '759 patent, Intel's only theory was anticipation by the Yonah processor ("Yonah"). The jury found Intel did not meet its burden to prove anticipation by clear and convincing evidence. Intel now seeks JMOL, saying that "a reasonable jury could only conclude" Intel proved anticipation. D.I. 591 at 14. Intel is wrong.

For example, there was far more than substantial evidence sufficient for a reasonable jury to find Intel did not prove Yonah included "a ***programmable clock controller*** having an ***embedded*** computer program ***therein … including instructions***" (claim 14), or "a ***clock controller coupled to*** the arbiter and ***coupled to*** the first master device" (claim 18). PTX-5. Intel had the burden of proof, yet Intel's witnesses failed to ever articulate ***what*** in Yonah allegedly meets these limitations, or ***how*** they are allegedly met. They just provided bare assertions that Yonah purportedly had a "programmable clock controller" or "clock controller," while failing to ever clearly identify what (if anything) they were pointing to. *E.g.*, 2/26 Tr. [Rotem] 1061:23-24, 1063:24-1064:16, 1083:10-19, 1124:15-24, 1130:19-1131:19, 1134:3-1135:4; 2/26 Tr. [Grunwald] 1221:2-9, 1224:12-1225:7 (citing D-267.11), 1226:1-1227:6 (citing D-267.8), 1229:11-1230:3 (citing D-281.11). Indeed, on cross-examination, Intel's expert responded with a practically unintelligible non-answer:

> Q. ***What are you pointing to*** as the ***programmable clock controller*** in Yonah?
> A. So it combines all of the things shown on this slide plus microcode that is used to provide results to this slide, plus microcode that manipulates the GV3 stepper, which I think is what the next slide describes.
> Q. So we would have to look at more than just that to see the programmable clock controller?
> A. Yes.

3/1 Tr. [Grunwald] 1338:12-20 (citing D-267.11 and DDX-10.71). Intel's witnesses also failed to explain how any alleged "programmable clock controller" in Yonah allegedly meets the limitations

of "having an embedded computer program therein" (claim 14) or being "coupled to the arbiter and coupled to the first master device" (claim 18). PTX-5; *see, e.g.*, 2/26 Tr. [Grunwald] 1301:17-1302:8 (agreeing it needs "to be programmable and have embedded in it a computer program").

"Courts grant JMOL for the party bearing the burden of proof only in extreme cases, when the party bearing the burden of proof has established its case by evidence that the jury would not be at liberty to disbelieve and the only reasonable conclusion is in its favor." *Mentor H/S, Inc. v. Medical Device Alliance, Inc.*, 244 F.3d 1365, 1375 (Fed. Cir. 2001). Here, Intel failed to meet its burden of proof before VLSI even began its rebuttal case. The Court could end its analysis here.

In rebuttal, Dr. Conte provided the jury even more reason to reject Intel's flawed theory. "Yonah is the old approach" to speed changes, he explained, whereas the '759 patent and Intel's infringing Skylake processors use "the new approach." 3/1 Tr. [Conte] 1403:17-25; *see also* 2/26 Tr. [Grunwald] 1263:15-24 (agreeing "Yonah was the old way," and "Skylake was the new way." "Yonah used SpeedStep," whereas "Skylake used Speed Shift."); *id.* at 1172:3-1173:8, 1176:7-20. In the '759 patent's new approach, speed changes are controlled by a "computer-in-a-computer," *i.e.*, a "programmable clock controller with an embedded computer program." 3/1 Tr. [Conte] 1405:19-25. In Intel's infringing Skylake processors, the "programmable clock controller" includes the "PCU." *Id.* at 1411:1-21. In contrast, "[i]n Yonah it was the operating system" making speed control decisions. 3/1 Tr. [Conte] 1406:2-1407:5; *see also, e.g.*, 2/26 Tr. [Grunwald] 1221:2-9; 2/26 Tr. [Rotem] 1061:23-1064:16, 1083:10-19, 1124:15-24. Yonah did not include a "PCU," nor any other "programmable clock controller" with "an embedded computer program" as required by the '759 patent claims. 3/1 Tr. [Conte] 1411:1-1417:20; PDX5.1-5.10.[4] The jury's rejection of

[4] *See also, e.g.*, 2/26 Tr. [Grunwald] 1275:7-15 (conceding that "the old legacy Yonah processor did not have a PCU," the "Skylake processors do have a PCU," and "the PCU is a programmable clock controller having an embedded computer program"); 2/26 Tr. [Rotem] 1103:19-1104:16 (conceding that Yonah "did not have a hardware controller").

Intel's anticipation theory was thus well-supported, because "[i]n evaluating the evidence, the jury was free to disbelieve [Intel's witnesses] … and credit [Dr. Conte]." *i4i Ltd. Partnership v. Microsoft Corp.*, 598 F.3d 831, 848 (Fed. Cir. 2010) (affirming jury verdict of no anticipation).

Yet, having lost at trial, Intel now argues that "***the claim language and specification make clear that a hardware-based controller is not required and that software may be used***." D.I. 591 at 15. To the extent Intel is seeking a new (and incorrect) claim construction, Intel has waived that right by failing to request a construction before trial. *See Lazare Kaplan*, 628 F.3d at 1376. Intel has also "waived its right to bring a Rule 50(b) motion on this ground," *Isbell Records*, 774 F.3d at 867, as Intel did not make the argument it in its Rule 50(a) motion. *Compare* D.I. 591 at 15-16, *with* D.I. 551 at 13 (noting "Elements 14[D], 14[E]" in just one sentence without any argument).

In any event, Intel's new argument is contrary to the plain claim language. For example, claim 18 recites: "A ***system*** ***comprising***: a ***bus*** …; a ***first master device*** ***coupled to*** the bus; an ***arbiter*** ***coupled to*** the bus and ***coupled to*** the first master device …; and a ***clock controller*** ***coupled to*** the arbiter and ***coupled to*** the first master device …."PTX-5. This plain language indicates the "system" includes the listed hardware components, "coupled to" each other, including the "clock controller." *Id.* Claim 14 recites: "A ***system*** ***comprising***: a ***bus*** …; a ***first master device*** ***coupled to*** the bus …; and a ***programmable clock controller*** having an ***embedded*** computer program ***therein*** ...." PTX-5. This too indicates the "system" has the listed hardware, including "a ***programmable*** clock controller having an ***embedded*** computer program ***therein***." *Id.* Intel notes that "the claim language and specification make clear … that software may be used." D.I. 591 at 15. Of course it does—the "programmable clock controller" has software "embedded … therein." PTX-5, Cl. 14.

Further, Intel now appears to allege—for the first time—that the combination of the "***operating system [being] executed in the cores of Yonah***" meets these limitations. D.I. 591 at

15. ***But Intel presented no such argument at trial***. To the contrary, Intel distinguished the "operating system executing on the cores" from any "programmable clock controller." *E.g.*, 2/26 Tr. [Grunwald] 1221:2-9 ("So in Yonah the operating system executing on the cores would make a request …. to a clock controller …."); 2/26 Tr. [Rotem] 1124:15-24 ("In Yonah, the operating system ran on the core …. sends an explicit request to our programmable clock controller …."); *id.* at 1061:23-1064:16, 1083:10-19. ***Intel's Rule 50(a) motion also omitted this theory***, so Intel "has waived its right to bring a Rule 50(b) motion on this ground." *Isbell Records*, 774 F.3d at 867.

Finally, even if Intel had presented this theory, a reasonable jury could disagree that the "operating system [being] executed in the cores of Yonah" (D.I. 591 at 15) is a "programmable clock controller having an embedded computer program therein." PTX-5, Cl. 14. For example, a reasonable jury could find the cores do not have the operating system "embedded … therein," as the OS is stored off-chip and select instructions are loaded on demand. At minimum, reasonable jurors "might reach different conclusions," making JMOL improper. *Laxton*, 333 F.3d at 579.

III. INTEL'S MOTION FOR JMOL OF NO DAMAGES SHOULD BE DENIED

Intel seeks JMOL of no damages based on scattershot references to arguments in its Rule 59 motion and motions this Court has already rejected. For the reasons set forth in VLSI's *Daubert*, Rule 59, and other relevant oppositions, which VLSI hereby incorporates, JMOL should be denied.

First, Intel cites its own "real-world evidence," but ignores that the Court "must draw all reasonable inferences in favor of the nonmoving party" and "disregard all evidence favorable to the moving party that the jury is not required to believe." *Taylor-Travis*, 984 F.3d at 1112. The jury credited VLSI's evidence showing that, *e.g.*, nearly a billion Intel products obtained substantial performance and power savings benefits from Intel's infringement, and Intel made over [redacted] from those benefits. *See, e.g.*, 2/24 Tr. [Sullivan] 593, 653-74; PDX7.74-76.

Second, there is no support for Intel's speculation that the jury based its damages numbers on noncomparable agreements. A "jury is 'entitled to choose a damages award within the amounts advocated by the opposing parties.'" *Bayer Healthcare v. Baxalta Inc.*, 989 F.3d 964, 983 (Fed. Cir. 2021). Intel "does not really know if the jury based its award" on any agreement, and a source matching an awarded number does "not somehow put the number … off limits to the jury." *Spectralytics, Inc. v. Cordis Corp.*, 649 F.3d 1336, 1346-47 (Fed. Cir. 2011).

Third, Intel argues (i) that Dr. Sullivan failed to put relevant damages numbers in the record, which is false, and (ii) that the jury could not have credited Dr. Sullivan's testimony, with Intel rehashing arguments made in its Rule 59 motion and elsewhere. On (i), Dr. Sullivan refrained from saying certain numbers, like Intel's total revenues, ***only*** because Intel designated the numbers as confidential. But the numbers are in the record, including through exhibits like PTX-3903 and PTX-3904, which Dr. Sullivan walked the jury through. On (ii), VLSI incorporates the responses in Parts II & VII of its Opposition to Intel's Rule 59 Motion filed concurrently herewith.

Fourth, Intel repeats its Rule 59 entire market value rule argument, which mischaracterizes the facts and has been waived. *See* Rule 59 Opp., Part II.D. Dr. Sullivan did not apply a percentage royalty to Intel's total accused revenues, nor did he rely on those revenues to justify his result.

Finally, Intel references all *Daubert* motions it filed against VLSI's experts. For the reasons stated in VLSI's oppositions (D.I. 447-49, 454, 457), incorporated here, the Court already rejected Intel's arguments. Intel's failed *Daubert* attempts do not support JMOL of no damages. *See Ham Marine, Inc. v. Dresser Indus., Inc*., 72 F.3d 454, 461 (5th Cir.1995) ("Unless there was no credible evidence presented which might authorize the verdict, the jury's findings must stand.").

CONCLUSION

For the foregoing reasons, VLSI requests that the Court deny Intel's Rule 50(b) motion.

Respectfully submitted,

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CERTIFICATE OF SERVICE

A true and correct copy of the foregoing instrument was served or delivered electronically via email, to all counsel of record, on May 7, 2021.

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